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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,510	06/16/2000	Alan G. Wood	M4065.0184/P184	2407

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EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/594,510	Applicant(s) WOOD ET AL.	
	Examiner Chuong A Luu	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1, 5-6, 8, 10-12, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kata et al. (U.S. 5,897,337)

Kata discloses a method of manufacturing a semiconductor device by

(1); (11); (19) forming a layered assembly by attaching a wafer (40) and an electrode pad (41) to a dielectric layer (43) (see Figure 8A-8B);

connecting semiconductor devices in said semiconductor wafer (40) to ball grid arrays (44) on said dielectric layer (see Figure 8C);

subsequently, dicing said layered assembly (see column 7, lines 8-59);

(5) wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric layer (see Figure 8B);

(6) further comprising the step of electrically connecting said semiconductor devices to ball grid arrays (44) on said dielectric layer (43) (see Figure 8D);

(8) wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric layer (see column 7, lines 56-59);

(10) further comprising the step of providing an electrode pad in said layered assembly (see Figure 8A);

(12) wherein said forming step comprises the step of adhering said wafer (40) to said electrode pad (41) (see Figure 8A-8B);

Claims 2-3, 7, 13-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Heo et al. (US 5,858,815)

Kata teaches the above outlined features except for input/output devices. However, Heo discloses a method for fabricating semiconductor package by **(2)** further comprising the step of connecting said semiconductor devices to input/output devices on the dielectric layer; **(3)** wherein said testing is conducted through said input/output devices; **(18)** further comprising the step of testing said semiconductor devices through said ball grid arrays (see column 8, lines 32-56); **(7); (13); (14)** wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric layer (see columns 4, and 5, lines 49-57, and lines 1-17, respectively); **(15)**

wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric layer; **(16)** further comprising the step of connecting said traces to conductive vias extending through said dielectric layer (see columns 4, 5, and 6, lines 36-67, lines 1-67, and lines 1-63, respectively). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to apply an input/output device to conduct testing a semiconductor device.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Heo et al. (US 5,858,815), and further view of Lam (5,137,836)

Kata and Heo disclose everything above except for discarding one or more defective packages. Furthermore, Lam discloses a method of manufacturing a repairable multi-chip module by **(4)** further comprising the step of discarding one or more defective packages (see column 3, lines 1-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to discarding one or more defective chip to fabricate a semiconductor device.

Claims 9, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Mizuno et al. (US 6,077,757)

Kata discloses everything above except for using a saw. However, Mizuno discloses a method of forming chip semiconductor devices with **(9); (17)** wherein said dicing step is performed by a saw (see column 4, lines 17-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to dicing semiconductor chips by sawing.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Gaynes et al. (U.S. 6,165,885)

Kata teaches the above outlined features except for optically aligned. However, Gaynes discloses a method of making components with solder balls by **(20)** wherein said wafer is optically aligned with respect to said dielectric tape (see column 16, lines 18-29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings above by optically aligned semiconductor components to manufacture integrated circuit devices.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Gaynes et al. (U.S. 6,165,885), and further view of Huddleston et al. (U.S. 5,834,320)

Kata and Gaynes teach everything above except for magnetically aligned with a magnet ring. Furthermore, Huddleston discloses a method of assembling a semiconductor device using a magnet (see columns 7 and 8, lines 44-67 and lines 1-51, respectively). It would have been obvious to one having ordinary skill in the art at the

time the invention was made to magnetically aligned with a magnet ring to form a semiconductor device.

Claims 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Farnworth (U.S. 6,326,697 B1), and further view of Kobayashi et al. (U.S. 4,781,969)

Kata discloses a method of manufacturing a semiconductor device by

(35) connecting said semiconductor devices to respective ball grid arrays (44) located on said substrate (see Figure 8A-8B).

Kata teaches everything above except for using a flexible substrate, testing procedure and step of singulating packages.

However, Farnworht discloses integrated circuit with **(35).....** testing said semiconductor devices through said ball grid arrays (see column 5, lines 36-67); **(37)** further comprising the step of singulating packages from said wafer and said substrate (see column 5, lines 51-53).

Furthermore, Kobayashi discloses a printed circuit board with **(35).....** adhering said wafer to a flexible substrate (see column 1, lines 38-43). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Kata, Farnworth and Kobayashi to apply testing and singulating steps, to use a flexible substrate for fabricating a semiconductor device.

Claims 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. (U.S. 5,897,337) in view of Farnworth (U.S. 6,326,697 B1) and Kobayashi et al. (U.S. 4,781,969), and further view of Lam (5,137,836)

Kata, Farnworth and Kobayashi diclose everything above except for identifying defective packages. Furthermore, Lam discloses a method of manufacturing a repairable multi-chip module by **(36); (38)** further comprising the step of segregating defective packages from other packages (see column 3, lines 1-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to identifying one or more defective chip during fabrication of a semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

C. Everhart

CARROLL EVERHART
PRIMARY EXAMINER